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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,948	09/19/2003	Stephen J. Smith	174/161 Cont	7049

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,948	SMITH ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,15-18 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15-18,28* is/are rejected.

7)☒ Claim(s) *29-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 15-18 and 28-33 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al (US Patent No 5,537,601)

4. As per claim 1, Kimura et al teach

a central processing unit implemented on at least one programmable logic resource [fig. 35, 39, 40; CPU with a DSP or PL];

programmable logic coupled to the central processing unit, wherein the programmable logic is reconfigurable to optimize the ability of the computer system to handle a given application [Fig. 35, 39, 40; DSP or PL coupled to the CPU; col. 16, line 50 -- col. 17, line 9; clearly the programmable configured circuit is capable of conducting desired functions at very high speed and so it optimizes the ability of the computer system to handle a given application]; and

a secondary storage device that stores configuration data for the programmable logic, wherein the secondary storage device is a mass storage device [col. 8, lines 20-24; circuit configuration data from a storage medium such as a magnetic disk or optical disk].

5. As per claim 2, Kimura et al teach that the system further comprising non-volatile memory coupled to the programmable logic [Fig. 16, 18, 20, 39, 40; col. 8, lines 45-50].

6. As per claim 3, Kimura et al teach that the system further comprising random-access memory coupled to the programmable logic [Fig. 8; col. 6, lines 32-33; memory can be RAM].

7. As per claim 4, Kimura et al teach that the system further comprising input-output circuitry [Fig. 3, 39; data input/output line 32].

8. As per claim 15, Kimura et al teach swapping configuration data between a secondary storage device and the programmable logic resources during programmable logic resource allocation using a virtual logic manager, wherein the secondary storage device is a mass storage device [col. 4, lines 52-59; col. 5, lines 1-3; col. 8, lines 20-24, 50-56; col. 16, line 50 -- col. 17, line 9; moving configuration data from external memory or storage device of the host processor to programmable logic circuits ("swap in"), or vice versa ("swap out")].

9. As per claims 16-18, Kimura et al teach the reconfigurable computer includes a central processing unit may be implemented on or with one programmable logic device or a microprocessor or partially implemented on a microprocessor and that is partially implemented on a programmable logic device [fig. 35, 39, 40; CPU with a DSP or PL; different possible combinations].

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Kodosky et al (US Patent no 6,219,628 B1).

12. As per claim 28, Kodosky et al teach a method for managing resources in a computer that contains programmable logic resources that are reconfigurable to optimize the ability of the computer to handle a given application having multiple functions [col. 3, line 65 -- col. 4, line 14; col. 7, lines 57-62, 65-67; the computer includes programmable or reconfigurable hardware, for example, GPIB card, DAQ card, VXI card and FPGA] comprising:

during runtime [col. 4, lines 29-40; clearly the decision is made during the program execution], using a virtual computer operating system to determine whether to use a hardware implementation or a software implementation for a given one of the multiple functions of the given application [col. 3, line 65 -- col. 4, line 14; col. 4, lines 29-40; some portion are programmed in high level of programming complied into machine language for execution on a CPU and other portions are programmed to be hardware implemented; col. 9, lines 34-45; invention is operable for automatically creating hardware and software implementation of the given application; col. 12, lines 63-67].

Allowable Subject Matter

13. Claims 29-33 are objected to as being dependent upon a rejected base claim 28, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

14. Applicant's arguments with respect to claims 1-4, 15-18 and 28-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
January 4, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100